IN THE CLAIMS:

1. (Currently Amended) A method comprising:

reading a plurality of trace vectors from a file on a storage device;

identifying a subset of [[the]] trace vectors from the plurality of trace vectors ~~, wherein the subset of the trace vectors~~ to form [[forms]] a packet, wherein the packet is variable in length;

identifying a plurality of data fields within the packet based on a packet type; and

presenting each of the data fields as output to a user.

2. (Currently Amended) The method of claim 1, wherein reading the plurality of trace vectors includes reading the subset of [[the]] trace vectors into memory.

3. (Currently Amended) The method of claim 2, further comprising:

reading a second subset of [[the]] trace vectors into the memory, wherein the second subset of the trace vectors forms a second packet.

4. (Currently Amended) The method of claim 1, wherein the storage device is ~~a disk~~ one of an optical disk, a magnetic disk, and a memory within a computer.

5. (Currently Amended) The method of claim [[4]] 1, wherein ~~the disk is one of an optical disk and a magnetic disk~~ each of the plurality of trace vectors includes a clock bit, a plurality of data bits, and a flag bit.

6. (Currently Amended) The method of claim [[1]] 5, wherein ~~the storage device is memory within a computer~~ wherein the flag bit indicates one of a beginning of the packet when the flag bit is transitioned from zero to one, and an end of the packet when the flag bit is transitioned from one to zero.

7. (Original) The method of claim 1, further comprising:

reading the plurality of trace vectors from an item of test equipment; and

storing the plurality of trace vectors in the file.

8. (Original) The method of claim 7, wherein the item of test equipment is a logic analyzer.

9. (Original) The method of claim 8, wherein the logic analyzer is connected to a bus system.

10. (Original) The method of claim 7, wherein the item of test equipment reads the plurality of trace vectors in synchronization with a clock signal.

11. (Original) The method of claim 10, wherein the plurality of trace vectors are read in synchronization with rising edges and falling edges of the clock signal.

12. (Currently Amended) The method of claim [[1]] 6, wherein identifying the subset of [[the]] trace vectors includes monitoring [[a]] the flag bit to determine if the flag bit is transitioned from one of zero to one, and one to zero.

13. (Currently Amended) A computer program product in a computer readable medium, comprising instructions for:

reading a plurality of trace vectors from a file on a storage device;

identifying a subset of [[the]] trace vectors from the plurality of trace vectors to form ~~wherein the subset of the trace vectors forms~~ a packet, wherein the packet is variable in length;

identifying a plurality of data fields within the packet based on a packet type; and

presenting each of the data fields as output to a user.

14. (Currently Amended) The computer program product of claim 13, wherein reading the plurality of trace vectors includes reading the subset of [[the]] trace vectors into memory.

15. (Currently Amended) The computer program product of claim 14, comprising additional instructions for:

reading a second subset of the trace vectors into the memory, wherein the second subset of [[the]] trace vectors forms a second packet.

16. (Currently Amended) The computer program product of claim 13, wherein the storage device is ~~a disk~~ one of an optical disk, a magnetic disk, and a memory within a computer.

17. (Currently Amended) The computer program product of claim [[16]] 13, wherein ~~the disk is one of an optical disk and a magnetic disk~~ each of the plurality of trace vectors includes a clock bit, a plurality of data bits, and a flag bit.

18. (Currently Amended) The computer program product of claim [[13]] 17, wherein the ~~storage device is memory within a computer~~ flag bit indicates one of a beginning of the packet when the flag bit is transitioned from zero to one, and an end of the packet when the flag bit is transitioned from one to zero.

19. (Original) The computer program product of claim 13, comprising additional instructions for:

reading the plurality of trace vectors from an item of test equipment; and

storing the plurality of trace vectors in the file.

20. (Original) The computer program product of claim 19, wherein the item of test equipment is a logic analyzer.

21. (Original) The computer program product of claim 20, wherein the logic analyzer is connected to a bus system.

22. (Original) The computer program product of claim 19, wherein the item of test equipment reads the plurality of trace vectors in synchronization with a clock signal.

23. (Original) The computer program product of claim 22, wherein the plurality of trace vectors are read in synchronization with rising edges and falling edges of the clock signal.

24. (Currently Amended) The computer program product of claim [[13]] 18, wherein identifying the subset of [[the]] trace vectors includes monitoring [[a]] the flag bit to determine if the flag bit is transitioned from one of zero to one, and one to zero.

25. (Currently Amended) A data processing system comprising:

a bus system;

a processing unit connected to the bus system and including at least one processor;

memory connected to the bus system;

a set of instructions stored in the memory,

wherein the processing unit executes the set of instructions to perform the acts of:

reading a plurality of trace vectors from a file on a storage device;

identifying a subset of [[the]] trace vectors from the plurality of trace vectors ~~, wherein the subset of the trace vectors forms~~ to form a packet, wherein the packet is variable in length;

identifying a plurality of data fields within the packet based on a packet type; and

presenting each of the data fields as output to a user.

26. (Currently Amended) The data processing system of claim 25, wherein reading the plurality of trace vectors includes reading the subset of [[the]] trace vectors into the memory.

27. (Currently Amended) The data processing system of claim 26, wherein the processing unit executes the set of instructions to perform the additional acts of:

reading a second subset of [[the]] trace vectors into the memory, wherein the second subset of [[the]] trace vectors forms a second packet.

28. (Currently Amended) The data processing system of claim 25, wherein the storage device is ~~a disk~~ one of an optical disk, a magnetic disk, and a memory within a computer.

29. (Currently Amended) The data processing system of claim [[28]] 25, wherein ~~the disk is one of an optical disk and a magnetic disk~~ each of the plurality of trace vectors includes a clock bit, a plurality of data bits, and a flag bit.

30. (Currently Amended) The data processing system of claim [[25]] 29, wherein the ~~storage device is memory within a computer~~ flag bit indicates one of a beginning of the packet when the flag bit is transitioned from zero to one, and an end of the packet when the flag bit is transitioned from one to zero.

31. (Original) The data processing system of claim 25, wherein the processing unit executes the set of instructions to perform the additional acts of:

reading the plurality of trace vectors from an item of test equipment; and

storing the plurality of trace vectors in the file.

32. (Original) The data processing system of claim 31, wherein the item of test equipment is a logic analyzer.

33. (Original) The data processing system of claim 32, wherein the logic analyzer is connected to a bus system.

34. (Original) The data processing system of claim 31, wherein the item of test equipment reads the plurality of trace vectors in synchronization with a clock signal.

35. (Original) The data processing system of claim 34, wherein the plurality of trace vectors are read in synchronization with rising edges and falling edges of the clock signal.

36. (Currently Amended) The data processing system of claim [[25]] 30, wherein identifying the subset of [[the]] trace vectors includes monitoring [[a]] the flag bit to determine if the flag bit is transitioned from one of zero to one, and one to zero.